Abstract of the Disclosure

A method of fabricating a CMOS have self-aligned shallow trench isolation, includes preparing a silicon substrate; forming a gate stack; depositing a layer of first polysilicon; trenching the substrate by shallow trench isolation to form a trench; filling the trench with oxide; depositing a second layer of polysilicon wherein the top surface of the second polysilicon layer is above the top surface of the first polysilicon layer; depositing a sacrificial oxide layer having a thickness of at least 1.5X that of the first and second polysilicon layers; CMP the sacrificial oxide layer to the level of the upper surface of the second polysilicon layer; depositing a third layer of polysilicon; patterning and etching the gate stack; implanting ions to form a source region, a drain region and the polysilicon gate; and completing the CMOS structure.